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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,118	11/27/2001	Chuan-cheng Cheng	01-695/LS11P184	5362

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LSI Logic Corporation
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Milpitas, CA 95035

EXAMINER

RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 03/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

09/996,118

Applicant(s)

CHENG ET AL.

Examiner

Steven H. Rao

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 1-5 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Priority

The application has been filed without claiming priority to any preceding application. Therefore, the earliest currently available filing date is the U.S. filing date namely November 27, 2001.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-5 are, drawn to metal interconnect for integrated circuit device, classified in class 257, subclass 687.
- II. Claims 6-10 are, drawn to method of making an interconnect, classified in class 438, subclass 648.

Inventions Group I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the process as claimed can be used to make other and materially different product, namely forming an aluminum layer first and then forming a second copper layer thereon instead of the recited first copper layer and the second aluminum layer because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Timothy R. Croll, Esq. (Reg. No. 36,771) on March 12, 2002 a provisional election was made with traverse to prosecute the invention of Group II, claims 6-10.

Affirmation of this election must be made by applicant in replying to this Office action.

Claims 1-5 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over McTeer (U.S. Patent No. 5,939,788, herein after McTeer) and Robinson et al. (U.S. Patent No. 6,054,172, herein after Robinson)

With respect to claim 1, McTeer describes a method of fabricating a low resistance interconnect lines in an integrated circuit, including the steps of:

Patterning and etching a dielectric layer(McTERR, fig. 1 # 1 , col. 17 line 37) in an integrated circuit (McTERR fig. 1 col. 17, lines 50-55), filling the etched areas of the dielectric layer with a first conductive material (McTERR fig.1 # 3, col. 17 line 61), depositing a second conductive material on the first conductive material (McTERR fig. 2 # 5, col. 18 line 10), patterning and etching the second conductive material so that the second conductive material overlies areas filled with the first conductive material. interconnect (McTERR fig. # 9, col. 43-49, patterning and planarization).

McTeer does not specifically teach an etching step.

However, Robinson, a patent from the same filed of endeavor, in col.8 lines 13-18 describes an etching step as part of a patterning process to form a patterned aluminum layer that acts as a catalyst in preventing native oxidation formation from the titanium containing material thus allowing the deposition of Cooper layer with fewer impurities resulting in a low resistivity path through the titanium-containing and cooper layers within the IC , particularly in the interconnect structure of an IC where resistance to electrical current should be minimized.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include the Robinson's etching step as part of the patterning step in McTeer's process steps to form a patterned aluminum layer that acts as a catalyst in preventing native oxidation formation from the titanium containing material thus allowing the deposition of Cooper layer with fewer impurities resulting in a low resistivity path through the titanium-containing and cooper layers within the IC , particularly in the interconnect structure of an IC where resistance to electrical current should be minimized. (Robinson col. 8 lines 10-28).

With respect to claim 7, wherein the same mask that was used to pattern the dielectric layer is used to pattern the second conductive material (McTERR figs 1-5, col. 18 lines 15-25 and claim 7).

With respect to claim 8, wherein the first conductive material is cooper (McTERR fig. 1 # 3, col. 17, line 52) and the second conductive material is Aluminum (McTERR fig. 2 # 5, col. 18 lines 18-19).

With respect to claim 9, wherein a barrier material is deposited atop the cooper before the aluminum is deposited and patterned. (McTERR , fig. #4 , col. 18 line 9).

With respect to claim 10, wherein the thickness of the cooper and the thickness of the aluminum are adjusted to form an interconnect line having a first pre determined electrical resistance. (McTERR col. 1 lines 39-45 and col. 18 lines 60-65).

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-

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5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7722.

Steven H. Rao
Patent Examiner
March 13, 2002.



EDDIE LEE
SUPERVISORY PATENT EXAMINER
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